

Key Technology Corp.

FC1306T

Single Chip Controller for PC ATA Card Adapters

User's Programming Manual

(KTC Confidential)

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Revision Logs:

Features:

1. Host Interface:

1) Support PC Card ATA, Compact Flash and true IDE interface.
2) Fully compatible with PC Card Standard.
3) Fully compatible with CFA(Compact Flash Association) Standard.
4) Four PC Card ATA Modes:
   Common Memory Mapped.
   Contiguous I/O Mapped.
   Primary I/O(1Fx) Mapped.
   Secondary I/O(17x) Mapped.
5) Compatible with all PC Card Services and Socket Service.
6) Automatic sensing of PC Card ATA or true IDE host interface.
7) PIO, Multi-word DMA and Ultra DMA Host Data transfer Support.
8) Support 8-bit / 16-bit data transfer on host data bus.
9) Integrated PC Card attribute memory of 256 Bytes(CIS).
10) 4 PC Card function registers support.
11) Automatic wake up from power-down on host reset or command write.
12) Sector data transfers without microprocessor intervention.
13) ATAPI Interface (SSF-8020i and SFF-8070i)

2. Buffer Management:

1) Built-in 1Kx16 SRAM for Data Buffer.
2) Auto Data Movement based on the sector (256 words) size.
3) Multi-Address Pointer support for different device interface.

3. Error Correction Logic:

1) Data Interleave to 2 for each 256 Bytes.
2) Error Correction of 1 Byte random error per 128 Bytes of data.
3) Automatic on-the-fly, in-buffer error correction.
4) Built-in Standard SmartMedia Hardware ECC circuit.

4. Flash Memory Control:

1) Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically.
2) Flash Write Protect control support.
3) Support Samsung / Toshiba 16/32/64/128/256/512/1024/2048 Mbits NAND type flash memories.
4) Support Hitachi 64/128/256/512 Mbits AND type flash memories.
5) Support SmartMedia / SmartMedia 256 Card.
6) Support up to 8 devices.
7) 8-bit Flash Data I/O.

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5. MMC-Port for MMC/SD Card:

1) Fully compatible with MMC system specification 2.0.
2) Fully compatible with SD Memory Card specification 1.0.
3) Standard MMC Mode Interface support.
4) Standard SPI(Serial Programming Interface) Interface (option mode of MMC) for MMC(MultiMediaCard) Card.
5) Programmable Clock Rate (62.5KHz ~ 24MHz).
6) Microprocessor I/O transfer mode (High flexibility) or Automation transfer mode (High speed) Support.
7) Auto Command/Response CRC generation/check.
8) Auto Data CRC generation/check.
9) 2 Clock Lines support for twin-card operation.

6. MS-Port for Memory Stick /Memory Stick Pro™ Card:

1) Fully compatible with Memory Stick Standard -- Format Specification 1.2.
2) Programmable Clock Rate (62.5KHz ~ 24MHz).
3) Microprocessor I/O transfer mode (High flexibility) or Automatic transfer mode (High speed) Support.
4) Auto Interface waveform generation.
5) Auto Data CRC generation/check.
6) 2 Clock Lines support for twin-card operation.
7) Support Memory Stick Pro 1-bit / 4-bit data transfer.

7. ATA-Port for PC ATA Cards / CompactFlash Cards / IDE Devices / ATAPI Devices:

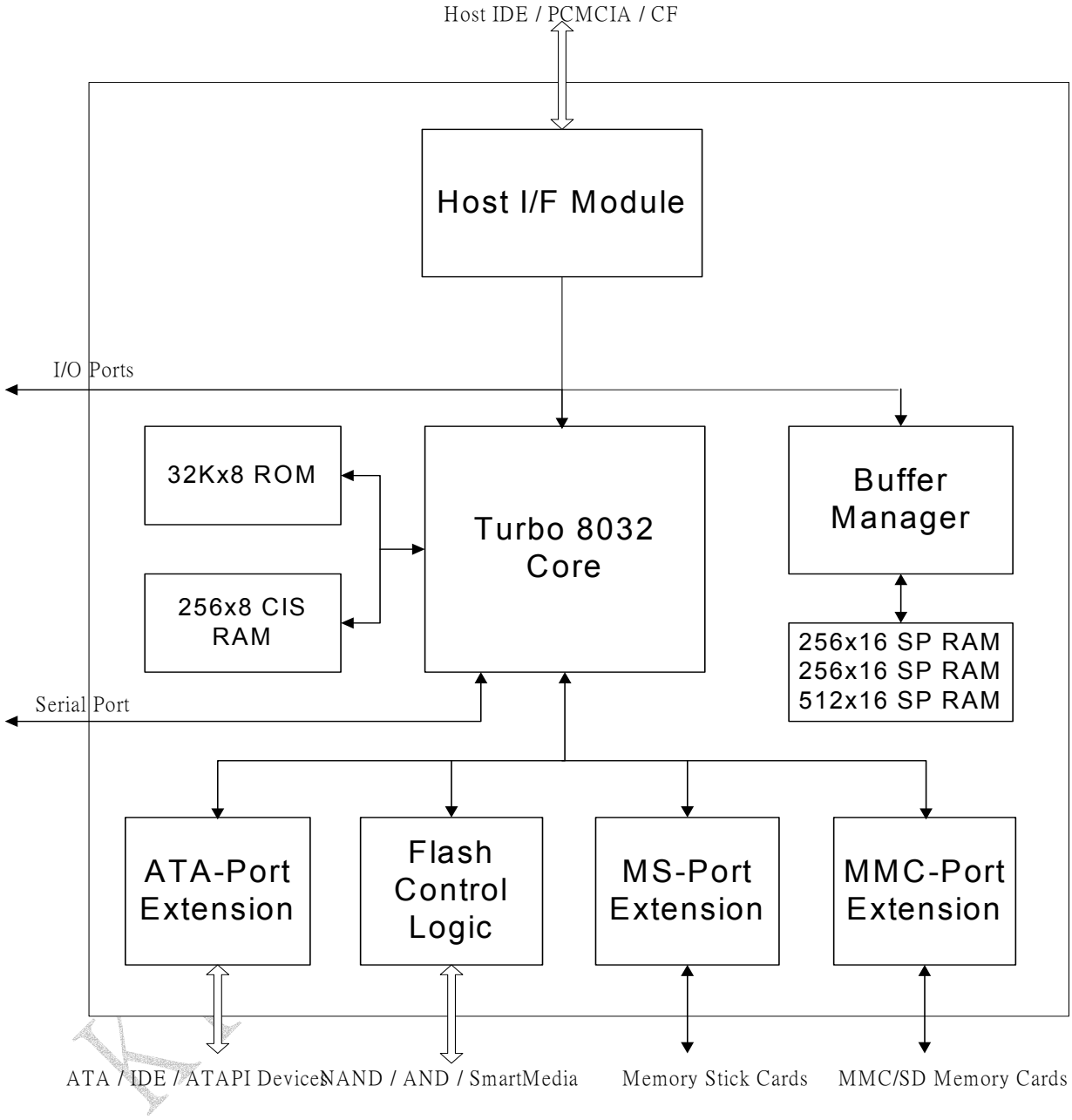
1) Support Standard PC Card ATA Host Interface.
2) Support Standard True IDE mode Host Interface.
3) Support ATAPI Packet Command interface.
4) Programmable Register Accessing Cycle Rate (Waveform timing).
5) 8-bit/16-bit Data bus selection for Task File Registers Accessing.
6) Full Task File Register Set Support.
7) Direct Buffer Accessing for Data or Command Packet Transferring.

8. Miscellaneous:

1) +5.5V ~ +3.0V wide range power supply.
2) Available in 100-lead/128-lead TQFP and QFP package.

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Functional Block Diagram:



6、Chip Mode Selection Table:

Pins Configuration			Chip Operation Description
DIS_IMP	IROMCS#	HIO16#	
0	0	X	Internal 8032 and Internal ROM
0	1	X	Internal 8032 and External ROM
1	1	X	External 8032 and External ROM
1	0	0	I8032 Test Mode
1	0	1	Internal RAM/ROM Test Mode

Internal RAM BIST Configurations

BIST1	BIST0	RAM	Size	INSTANCE NAME
0	0	CISRAM	256x8	CIS_BIST
0	1	XBUFFER	256x8x2	XY_BIST
		YBUFFER	256x8x2	
1	0	ZBUFFER	512x8x2	Z_BIST

External CLK	Internal /Double CLK	Internal 8032CLK	Host CLK	Buffer CLK	Flash/SM/ CLK	mmc/sd CLK	Memory Stick/Pro CLK	ata port CLK
45M(asic) 90M(fpga)	45M/90M	45M/ 22.5M	45M	45M	45M	90M	90M	45M/ 90M
			UDMA: 45M/90M					

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FC1306 Pins Assignment: total 100/128 pins

Bd.	Pin #		Type	Pin Name	Description
1	1	1	I/O	HD3	Host Data Bus 3
2	2	2	I/O	HD11	Host Data Bus 11
3	3	3	I/O	HD4	Host Data Bus 4
4	4		I/O	A15	Micro-processor Address Bus 15
5	5	4	I/O	HD12	Host Data Bus 12
6	6	5	I/O	HD5	Host Data Bus 5
7	7	6	I/O	HD13	Host Data Bus 13
8	8		I/O	A14	Micro-processor Address Bus 14
9	9	7	I/O	HD6	Host Data Bus 6
10	10	8	I/O	HD14	Host Data Bus 14
11	11	9	I/O	HD7	Host Data Bus 7
12	12		I/O	A13	Micro-processor Address Bus 13
13	13	10	I/O	HD15	Host Data Bus 15
14	14	11	P	I/O VDD	VDD
15	14	11	P	I/O VDD	VDD
16	15	12	I	CE1#	Card Enable 1. (Pull up 50KΩ)
17	16		I/O	A12	Micro-processor Address Bus 12
18	17	13	I	CE2#	Card Enable 2. (Pull up 50KΩ)
19	18	14	I O	HA10 DA10	Host PCMCIA: PC Card ATA Address 10 Device PCMCIA: PC Card ATA Address 10
20	19	15	I I	HOE# IDE_CS#	Host Output Enable. (Pull up 50KΩ) Host True IDE interface Select
21	20		I/O	A11	Micro-processor Address Bus 11
22	21	16	P	GND	I/O Ground
23	21	16	P	GND	I/O Ground
25	22	17	I	ENCLK	ENCLK=’1’,ExtCLK . ENCLK=’0’, IntCLK
26	23	18	I	HIOR#	Host I/O Read. (Pull up 50KΩ)
27	24	19	I	HIOW#	Host I/O Write. (Pull up 50KΩ)
28	25	20	I O	HA9 DA9	Host PCMCIA: PC Card ATA Address 9 Device PCMCIA: PC Card ATA Address 9
29	26		I/O	A10	Micro-processor Address Bus 10
30	27	21	I O	HA8 DA8	Host PCMCIA: PC Card ATA Address 8 Device PCMCIA: PC Card ATA Address 8
31	28	22	I O	HWE# DOE#	Host Write Enable. (Pull up 50KΩ) Device Output Enable
32	29		I/O	A9	Micro-processor Address Bus 9
33	30	23	P	VDD	I/O VDD
34	30	23	P	VDD	I/O VDD
35	31	24	O I O T	HRDY Mas/Sla HIRQ# HIRQ	Memory: PC Card is Ready Select Mas/Sla PC Card I/O: Host Interrupt Request. True IDE: Host Interrupt Request.
36	32	25	I O	HA7 DA7	Host PCMCIA: PC Card ATA Address 7 Device PCMCIA: PC Card ATA Address 7
37	33	26	I O	HA6 DA6	Host PCMCIA: PC Card ATA Address 6 Device PCMCIA: PC Card ATA Address 6
38	34	27	I	HRST	Host Reset.(Schmit)
39	35		I/O	A8	Micro-processor Address Bus 8
40	36	28	I O	HA5 DA5	Host PCMCIA: PC Card ATA Address 5 Device PCMCIA: PC Card ATA Address 5
41	37	29	O	WAIT#	Host Wait. (Pull up 50KΩ)
42	38		I/O	A7	Micro-processor Address Bus 7
43	39	30	I O	HA4 DA4	Host PCMCIA: PC Card ATA Address 4 Device PCMCIA: PC Card ATA Address 4

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44	**40**	**31**	O T	INPACK# DMARQ	PC Card: Input Acknowledge DMA Acknowledge as ATA DMA
45	**41**	**32**	I O	HA3 DA3	Host PCMCIA: PC Card ATA Address 3 Device PCMCIA: PC Card ATA Address 3
46	**42**		I/O	A6	Micro-processor Address Bus 6
47	**43**	**33**	I I	REG# DMACK#	Attribute Memory Access (Pull up 50KΩ) Host IDE: DMA Acknowledge
48	**44**	**34**	I	HA2	Host Address Bus 2
49	**45**	**35**	O O I/O	BVD2 SPKR# DASP#	Memory: Battery Voltage Detect 2. PC Card I/O: Audio Speaker Drive Active/Slave Present. (Pull up 50KΩ)
50	**46**		I/O	A5	Micro-processor Address Bus 5
51	**47**	**36**	I	HA1	Host Address Bus 1
52	**48**		P	VDD	I/O VDD (3.3V)
52	**48**		P	VDD	I/O VDD (3.3V)
53	**49**	**37**	O O I/O	BVD1 STSCHG# PDIAG#	Memory: Battery Voltage Detect 1. PC Card I/O: Status Changed. Drive Passed Diagnostics. (Pull up 50KΩ)
54	**50**		I/O	A4	Micro-processor Address Bus 4
55	**51**	**38**	I	HA0	Host Address Bus 0
56	**52**	**39**	I/O	HD8	Host Data Bus 8
57	**53**	**40**	I/O	HD0	Host Data Bus 0
58	**54**		I/O	A3	Micro-processor Address Bus 3
59	**55**	**41**	I/O	HD9	Host Data Bus 9
60	**56**	**42**	I/O	HD1	Host Data Bus 1
61	**57**	**43**	P	VDD	I/O VDD
62	**57**	**43**	P	VDD	I/O VDD
63	**58**		I/O	A2	Micro-processor Address Bus 2
64	**59**	**44**	I/O	HD10	Host Data Bus 10
65	**60**	**45**	I/O	HD2	Host Data Bus 2
66	**61**	**46**	O O T	WP IOIS16# IOIS16#	Memory: Card is Write Protected PC Card I/O: Host Data I/O is 16-bit. Host IDE: Host Data I/O is 16-bit.
67	**62**	**47**	I	IROMCS#	Internal ROM Chip Select (Pull down 50KΩ)
68	**63**	**48**	I	DIS_IMP	Disable Internal 8032 (Pull down 50KΩ)
69	**64**	**49**	P	GND	I/O Ground
71	**64**	**49**	P	GND	I/O Ground
72	**65**	**50**	P	GND	Analog Ground
73	**66**	**51**	A	VHV	Analog VCC for 3.3V Regulator
74	**67**	**52**	A	V33_OUT	3.3V Regulation Output
75	**68**	**53**	P	AVDD	Analog OSC VDD.
76	**69**	**54**	A	AGND	Analog Ground
77	**69**	**54**	A	AGND	Analog Ground
78	**70**	**55**	I	XTAL1	Crystal Port 1, Clock input
79	**71**	**56**	O	XTAL2	Crystal Port 2
80	**72**	**57**	P	VDT	
81	**73**	**58**	P	VDT Power	
82	**74**	**59**	P	GND	I/O Ground
83	**74**	**59**	P	GND	I/O Ground
84	**75**		I/O	A1	Micro-processor Address Bus 1
85	**76**	**60**	I/O	IOP0	Internal 8032 P1.0 (Pull up 50KΩ)
86	**77**	**61**	I/O	IOP1	Internal 8032 P1.1
87	**78**		I/O	A0	Micro-processor Address Bus 0
88	**79**	**62**	I/O	IOP2	Internal 8032 P1.2
89	**80**	**63**	I/O	IOP3	Internal 8032 P1.3
90	**81**	**64**	I	RESET#	Chip Reset. (Schmidt)
91	**82**	**65**	P	GND	I/O Ground
92	**82**	**65**	P	GND	I/O Ground

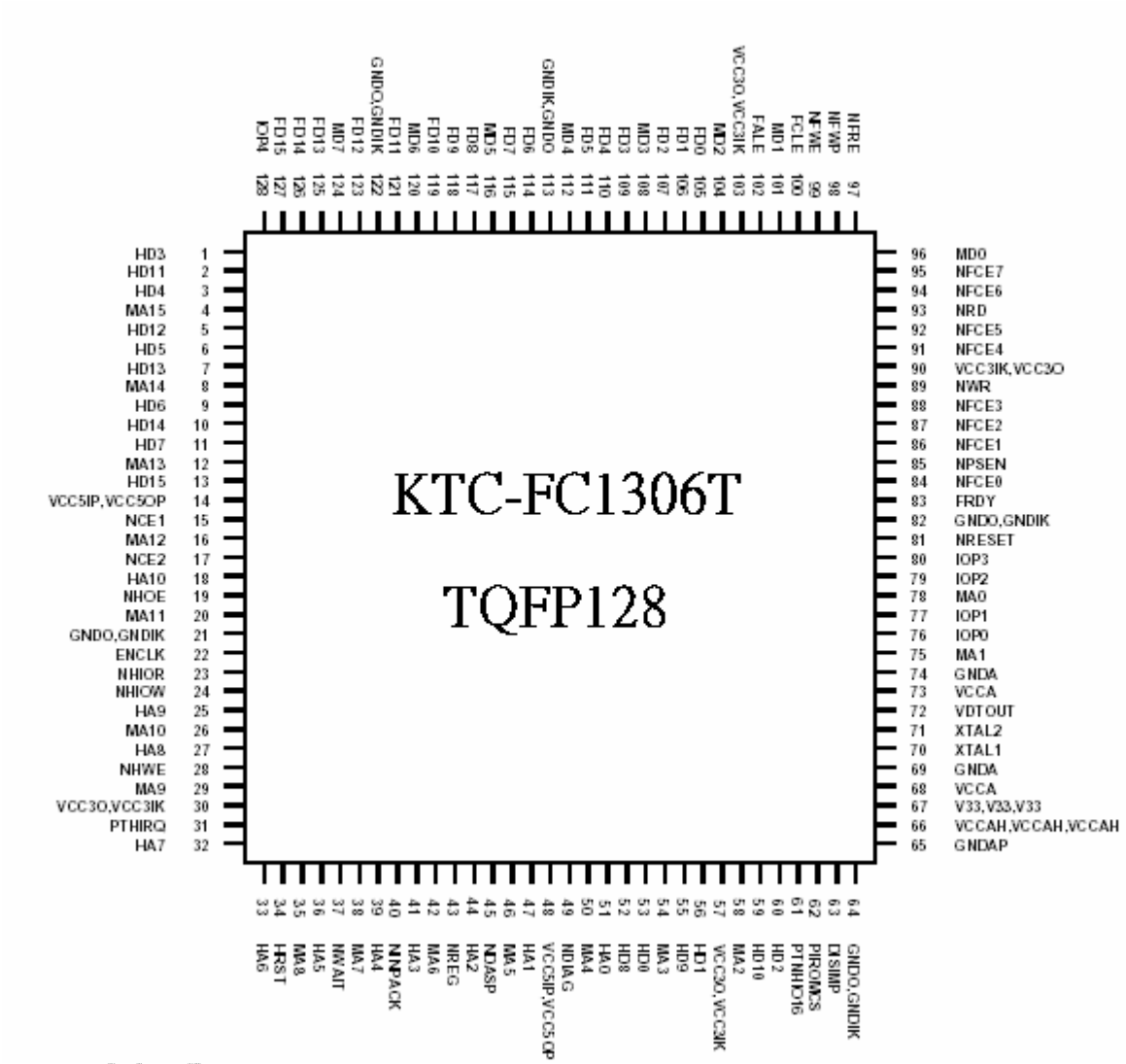
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93	**82**	**65**	P	GND	I/O Ground
94	**83**	**66**	I	FARDY	Flash A-Port Ready/Busy- (Schmit, Pull up 50KΩ)
95	**84**	**67**	O	FCE0#	Flash Device Select 0
96	**85**		I O	PSEN# PSEN#	ROM Output Enable (Pull up 50KΩ), External uP (Input) / Internal uP (output)
97	**86**	**68**	O O	FCE1# NDREG	Flash Device Select 1 ATA-Port NDREG
98	**87**	**69**	O O O	FCE2# MSCLK1 DA1	Flash Device Select 2 Memory Stick: Synchronous Clock 1 Device PCMCIA: PC Card ATA Address 1
99	**88**	**70**	O O O	FCE3# MCLK1 DA2	Flash Device Select 3 MMC/SD: Synchronous Clock 1 Device PCMCIA: PC Card ATA Address 2
100	**89**		I O	MWR# MWR#	Micro-processor Write (Pull up 50KΩ), External (Input) / Internal (output)
101	**90**	**71**	P	VDD	I/O VDD
102	**90**	**71**	P	VDD	I/O VDD
103	**91**	**72**	O O	FCE4# MSCLK0	Flash Device Select 4 Memory Stick: Synchronous Clock 0
104	**92**	**73**	O O	FCE5# MCLK0	Flash Device Select 5 MMC/SD: Synchronous Clock 0
105	**93**		I O	MRD# MRD#	Micro-processor Read (Pull up 50KΩ), External (Input) / Internal (output)
106	**94**	**74**	O O	FCE6# AT_CE1#	Flash Device Select 6 ATA-Port: Card Enable 1
107	**95**	**75**	O O	FCE7# AT_CE2#	Flash Device Select 7 ATA-Port: Card Enable 2
108	**96**		I/O	MD0	Micro-processor Data Bus 0
109	**97**	**76**	O O O	FARE# FAOE# AT_IOR#	NAND: Flash A-Port Read Enable AND: Flash A-Port Output Enable ATA-Port: IO read strobe
110	**98**	**77**	O O O	FWP# DWE# FRES#	NAND: Flash Write Protect Device Write Enable AND: Flash Reset
111	**99**	**78**	O O	FAWE# AT_IOW#	Flash A-Port Write Enable Strobe ATA-Port: IO write strobe.
112	**100**	**79**	O O	FCLE FCDE#	NAND: Flash Command Latch Enable AND: Flash Command Data Enable
113	**101**		I/O	MD1	Micro-processor Data Bus 1
114	**102**	**80**	O O O	FAALE FASC DA0	NAND: Flash A-Port Address Latch Enable AND: Flash A-Port Serial Clock Device PCMCIA: PC Card ATA Address 0
115	**103**	**81**	P	VDD	I/O VDD.
116	**103**	**81**	P	VDD	I/O VDD.
117	**104**		I/O	MD2	Micro-processor Data Bus 2
118	**105**	**82**	I/O I/O	FAD0 ATD0	Flash A-Port Data Bus 0 (Pull up 50KΩ) ATA-Port: Data Bus 0
119	**106**	**83**	I/O I/O	FAD1 ATD1	Flash A-Port Data Bus 1 (Pull up 50KΩ) ATA-Port: Data Bus 1
120	**107**	**84**	I/O I/O O	FAD2 ATD2 MS_BS	Flash A-Port Data Bus 2 (Pull up 50KΩ) ATA-Port: Data Bus 2 MS-Port: Bus State
121	**108**		I/O	MD3	Micro-processor Data Bus 3
122	**109**	**85**	I/O I/O I/O	FAD3 ATD3 MS_SD0	Flash A-Port Data Bus 3 (Pull up 50KΩ) ATA-Port: Data Bus 3 MS-Port: SDIO of Memory Stick Cards
123	**110**	**86**	I/O I/O I/O	FAD4 ATD4 MS_SD1	Flash A-Port Data Bus 4 (Pull up 50KΩ) ATA-Port: Data Bus 4 MS-Port: SDIO of Memory Stick Cards

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124	**111**	**87**	I/O I/O I/O	FAD5 ATD5 MS_SD2	Flash A-Port Data Bus 5 (Pull up 50KΩ) ATA-Port: Data Bus 5 MS-Port: SDIO of Memory Stick Cards
125	**112**		I/O	MD4	Micro-processor Data Bus 4
126	**113**	**88**	P	CGND	Core Ground
127	**113**	**88**	P	CGND	Core Ground
128	**114**	**89**	I/O I/O I/O	FAD6 ATD6 MS_SD3	Flash A-Port Data Bus 6 (Pull up 50KΩ) ATA-Port: Data Bus 6 MS-Port: SDIO of Memory Stick Cards
129	**115**	**90**	I/O I/O	FAD7 ATD7	Flash A-Port Data Bus 7 (Pull up 50KΩ) ATA-Port: Data Bus 7
130	**116**		I/O	MD5	Micro-processor Data Bus 5
131	**117**	**91**	I/O	ATD8	ATA-Port: Data Bus 8
132	**118**	**92**	I/O	ATD9	ATA-Port: Data Bus 9
133	**119**	**93**	I/O I/O	ATD10 MMC_DAT3	ATA-Port: Data Bus 10 MMC mode: MMC Data 3 Line.
134	**120**		I/O	MD6	Micro-processor Data Bus 6
135	**121**	**94**	I/O I/O	ATD11 MMC_DAT2	ATA-Port: Data Bus 11 MMC mode: MMC Data 2 Line.
136	**122**	**95**	P	GND	I/O Ground
137	**122**	**95**	P	GND	I/O Ground
138	**122**	**95**	P	GND	I/O Ground
139	**123**	**96**	I/O I/O	ATD12 MMC_DAT1	ATA-Port: Data Bus 12 MMC mode: MMC Data 1 Line.
140	**124**		I/O	MD7	Micro-processor Data Bus 7
141	**125**	**97**	I/O	ATD13	ATA-Port: Data Bus 13
142	**126**	**98**	I/O I/O O	ATD14 MMC_CMD SPI_DO	ATA-Port: Data Bus 14 MMC Mode: MMC Command Line. SPI-Port: SPI Data output
143	**127**	**99**	I/O I/O I	ATD15 MMC_DAT0 SPI_DI	ATA-Port: Data Bus 15 MMC mode: MMC Data Line. SPI-Port: SPI Data input
144	**128**	**100**	I/O O O	IOP4 HINT SDIO	Internal 8032 P1.4 External 32 mode :HINT Memory Stick SDIO

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TQFP128
1 HD3
2 HD11
3 HD4
4 MA15
5 HD12
6 HD5
7 HD13
8 MA14
9 HD6
10 HD14
11 HD7
12 MA13
13 HD15
14 VCC5IP,VCC5OP
15 NCE1
16 MA12
17 NCE2
18 HA10
19 NHOE
20 MA11
21 GNDO,GNDIK
22 ENCLK
23 NHIOR
24 NHIOW
25 HA9
26 MA10
27 HA8
28 NHWE
29 MA9
30 VCC3O,VCC3IK
31 PTHIRQ
32 HA7
33 HA6
34 HRST
35 MA8
36 HA5
37 NWAIT
38 MA7
39 HA4
40 NINPACK
41 HA3
42 MA6
43 NREG
44 HA2
45 NDASP
46 MA5
47 HA1
48 VCC5IP,VCC5OP
49 NDIAG
50 MA4
51 HA0
52 HD8
53 HD0
54 MA3
55 HD9
56 HD1
57 VCC3O,VCC3IK
58 MA2
59 HD10
60 HD2
61 PTNHD16
62 PIROMCS
63 CKSIMP
64 GNDO,GNDIK
65 GNDAP
66 VCCAH,VCCAH,VCCAH
67 V33,V33,V33
68 VCCA
69 GNDA
70 XTAL1
71 XTAL2
72 VDTOUT
73 VCCA
74 GNDA
75 MA1
76 IOP0
77 IOP1
78 MA0
79 IOP2
80 IOP3
81 NRESET
82 GNDO,GNDIK
83 FRDY
84 NFCE0
85 NPSEN
86 NFCE1
87 NFCE2
88 NFCE3
89 NWR
90 VCC3IK,VCC3O
91 NFCE4
92 NFCE5
93 NRD
94 NFCE6
95 NFCE7
96 MD0
97 NFRE
98 NFWP
99 NFWE
100 FCLE
101 MD1
102 FALE
103 VCC3O,VCC3IK
104 MD2
105 FD0
106 FD1
107 FD2
108 MD3
109 FD3
110 FD4
111 FD5
112 MD4
113 GNDIK,GNDO
114 FD6
115 FD7
116 MD5
117 FD8
118 FD9
119 FD10
120 MD6
121 FD11
122 GNDO,GNDIK
123 FD12
124 MD7
125 FD13
126 FD14
127 FD15
128 IOP4

Electrical Specifications:

1. DC Characteristics:

Absolute Maximum Rating

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Core power supply	-0.3 to 3.9	V
V_{CC5}	Power supply of 5V I/O	-0.3 to 6.0	V
V_{IN3}	Input voltage of 3.3V I/O	-0.3 to Vcc+0.3	V
	Input voltage of 3.3V I/O with 5V tolerance	-0.3 to Vcc5+0.3	V
V_{IN5}	Input voltage of 5V I/O	-0.3 to Vcc5+0.3	V
V_{out3}	Output voltage of 3.3V I/O	-0.3 to Vcc+0.3	V
V_{out5}	Output voltage of 5V I/O	-0.3 to Vcc5+0.3	V
T_{STG}	Storage temperature	-40 to 150	℃

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the optional sections of this datasheet. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Core power supply		3.0	3.3	3.6	V
V_{CC5}	Power supply of 5V I/O	Commercial	4.75	5.0	5.25	V
		Industrial	4.5	5.0	5.5	V
V_{IN3}	Input voltage of 3.3V I/O		0	3.3	3.6	V
	Input voltage of 3.3V I/O with 5V tolerance		0	3.3	5.25	V
V_{IN5}	Input voltage of 5V I/O		0	5	5.25	V
T_j	Junction operating temperature	Commercial	0	25	115	℃
		Industrial	-40	25	125	℃

Leakage Current and Capacitance

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IN}	Input leakage current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN3}	3.3V input capacitance			2.8		pF
C_{OUT3}	3.3V output capacitance			3.3		pF
C_{BID3}	3.3V bi-directional capacitance			4		pF
C_{IN5}	5V input capacitance			4		pF
C_{OUT5}	5V output capacitance			4.4		pF
C_{BID5}	5V bi-directional capacitance			4.4		pF

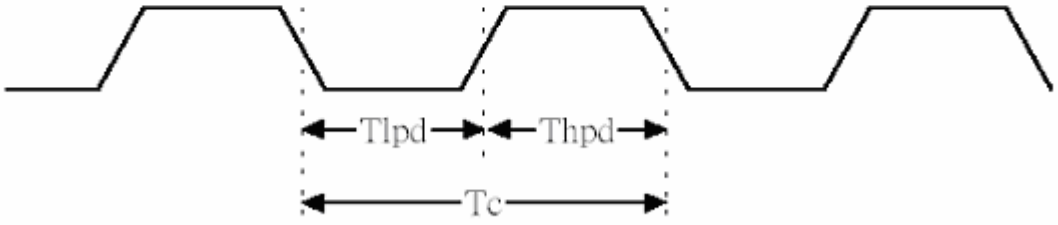
DC Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VCCK	Core power supply	Core area	3.0	3.3	3.6	V
VCC3I	Power supply	3.3V I/O	3.0	3.3	3.6	V
VCC3O	Power supply		3.0	3.3	3.6	V
V_{il}	Input low voltage	CMOS			0.3*Vcc	V
V_{ih}	Input high voltage		0.7*Vcc			V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	0.9	1.2		V
V_{t+}	Schmitt trigger positive going threshold voltage			2.1	2.5	V
V_{t-}	Schmitt trigger negative going threshold voltage	LVTTL	0.9	1.1		V
V_{t+}	Schmitt trigger positive going threshold voltage			1.6	1.9	V
V_{ol}	Output low voltage	I_{ol} = 2 ~24 mA			0.44(2)	V
V_{oh}	Output high voltage	I_{oh} = -2 ~ -24 mA	2.4			V
R_{pu}	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
R_{pd}	Input pull-down resistance	V_{in} = VCC3I	40	75	190	KΩ

2. AC Characteristics:

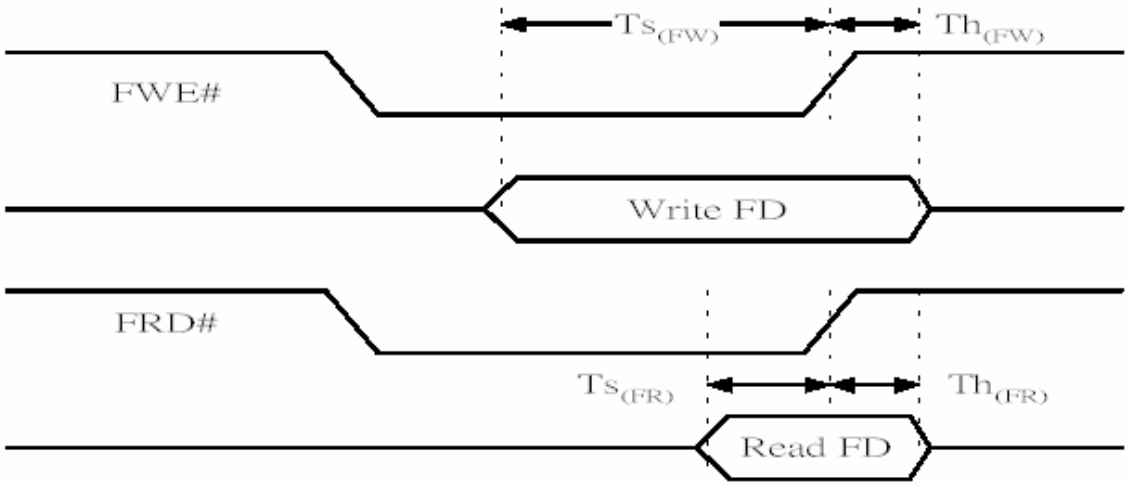
2.1 System clock timing:

Sym.	Description	Min.	Typ.	Max.	Unit
Tc	Clock cycle time		22.5		ns
Tlpd	Clock low pulse duration	0.4Tc		0.6Tc	ns
Thpd	Clock high pulse duration	0.4Tc		0.6Tc	ns

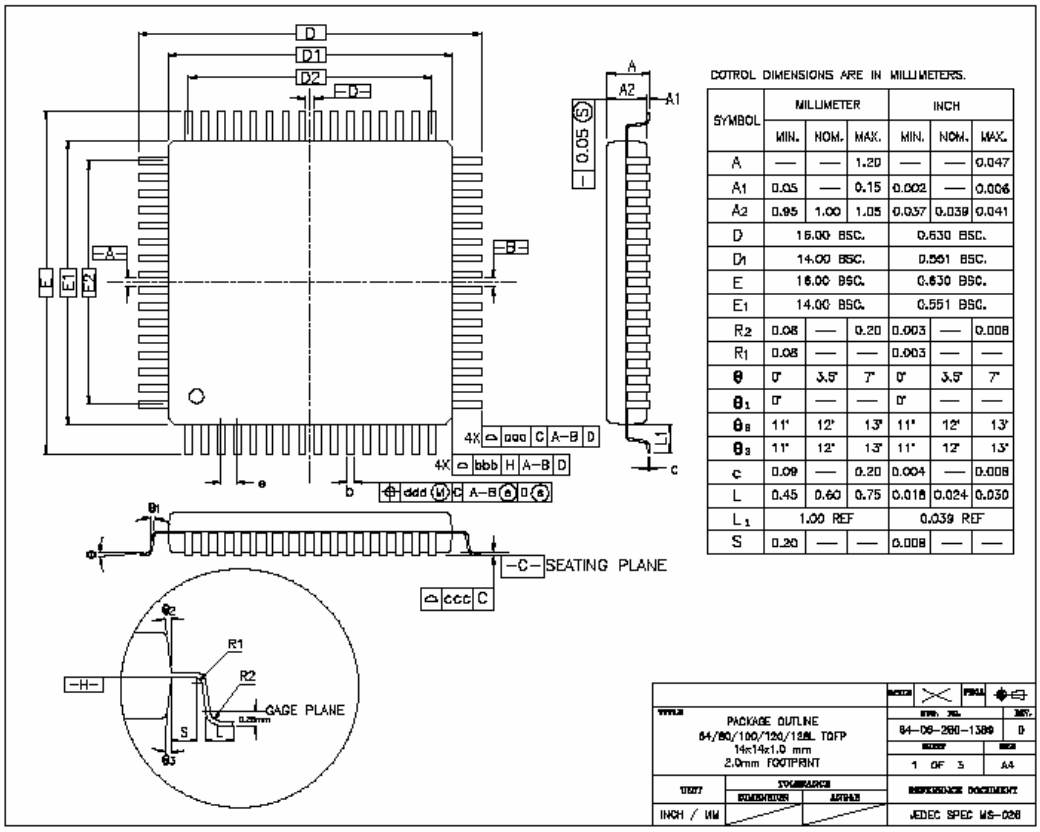


2.2 Flash Read/Write timing:

Sym.	Description	Min.	Typ.	Max.	Unit
$Tc_{(F)}$	Flash Read / Write cycle time		100		ns
$Ts_{(FW)}$	FD set up time of FWE#	80			ns
$Th_{(FW)}$	FD hold time of FWE#	40			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns



KTC Confi



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

TITLE: PACKAGE OUTLINE 64/80/100/120/128L TQFP 14x14x1.0 mm 2.0mm FOOTPRINT		DWG. NO.	REV.
		94-08-280-1389	D
		SHEET 1 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

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SYMBOL	64L						80L						100L						120L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.22	0.30	0.38	0.009	0.012	0.015	0.17	0.20	0.27	0.007	0.008	0.011	0.13	0.16	0.23	0.005	0.006	0.009
e	0.80 BSC.			0.031 BSC.			0.65 BSC.			0.026 BSC.			0.50 BSC.			0.020 BSC.			0.40 BSC.			0.016 BSC.		
D2	12.00			0.472			12.35			0.486			12.00			0.472			11.60			0.457		
E2	12.00			0.472			12.35			0.486			12.00			0.472			11.60			0.457		
TOLERANCES OF FORM AND POSITION																								
aaa	0.20			0.008			0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.004			0.10			0.004			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.13			0.005			0.08			0.003			0.07			0.003		

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

TITLE: PACKAGE OUTLINE 64/80/100/120/128L TQFP 14x14x1.0 mm 2.0mm FOOTPRINT		DWG. NO.	REV.
		94-08-280-1389	D
		SHEET 2 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT: JEDEC SPEC MS-026	

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